REMARKS

Claims 1-16 and 19-21 are all the claims pending in the application.

By this Amendment, Applicant editorially amends claims 1-16. The amendments to claims 1-16 were made for reasons of precision of language and consistency, and do not narrow the literal scope of the claims and thus do not implicate an estoppel in the application of the doctrine of equivalents. In addition, Applicant cancels claims 17 and 18. Finally, in order to provide more varied protection, Applicant adds claims 19-21. Claims 19-21 are clearly supported throughout the specification, *e.g.*, see pages 7 and 8 of the specification.

Preliminary Matters

Applicant thanks the Examiner for acknowledging the claim to foreign priority and for confirming that the certified copy of the priority document was received. The Examiner is kindly asked to acknowledge acceptance of the drawing filed on October 19, 2001 and to acknowledge the receipt of the certified copy of the priority document in the next Office Communication.

Finally, the Examiner noted that the Declaration as filed on October 19, 2001 is defective because of a minor informality. A substitute Declaration is being prepared and will be filed with the USPTO soon.

Claim Rejections under 35 U.S.C. § 102

Claims 1, 6-12, 17, and 18 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,366,606 to Sriram (hereinafter "Sriram"). Applicant respectfully traverses this

rejection in view of the following comments. Claims 17 and 18 have been canceled. Therefore, this rejection is moot with respect to claims 17 and 18.

Of the remaining rejected claims, only claims 1 and 9-12 are independent. This response initially focuses on these independent claims. To begin, independent claim 1, among a number of unique features, recites a base station having "at least one digital signal processor configured to perform a symbol rate processing and at least parts of a chip rate processing." The Examiner alleges that claim 1 is related to a base station and is anticipated by Sriram. In particular, the Examiner alleges that Sriram's digital signal processor (hereinafter "DSP") is equivalent to the digital signal processor as set forth in claim 1 (see page 2 of the Office Action). Applicant respectfully disagrees with the Examiner. Applicant has carefully studied Sriram discussion of the DSP, which is not similar to having a processor configured to perform two types of processing, as set forth in claim 1.

For example, in the background of the invention, it is disclosed that a conventional base station has a DSP for performing symbol rate processing and FPGA for performing chip rate processing. When speech is transmitted, the data rate is low but the number of users can be high. The speech undergoes the chip rate processing. When transmitting internet data, the data rate is high but the number of users is low. The internet data undergoes the symbol rate processing. The base station should be equipped to accommodate both situations, when the number of users is high or when the data transmission rate is high. The two situations, however, will never occur simultaneously. Consequently, unused FPGAs or DSPs are always present in the base station. In the present invention as recited in claim 1, however, at least one digital signal processor is

configured to perform a symbol rate processing and at least parts of a chip rate processing. Thereby, over-dimensioning of the base station is lessened.

In general, Sriram teaches a digital transmissions receiver system which includes a digital transmissions receiver and a correlation co-processor. The correlation co-processor performs correlation operations at the request of the digital transmissions receiver. Power consumption in the correlation co-processor is reduced by performing the requested correlation operations in stages. The number of stages used is inversely proportional to the number of gates required to implement the correlation function. Thus, the more stages used, the fewer gates are required. This, in turn, provides lower power consumption as compared with a non-staged implementation of the correlation function. Various types of correlations may be performed as indicated by correlation control signals received from the digital transmissions receiver. A correlation controller, included in the correlation co-processor, keeps track of the various stages and with the data appropriate to each stage. When all of the stages necessary to process a particular piece of data are complete, the <u>recovered symbol rate data is stored in an output buffer to await symbol rate processing by the digital transmissions receiver</u> (col. 1, lines 30 to 55).

In particular, Sriram teaches a digital receiver 10, which is implemented on a DSP (col. 2, lines 31 to 33). The digital receiver 10 interfaces with a programmable correlator co-processor 12. The correlator co-processor is not located in the receiver but is a separate unit that communicates with the receiver. It is this correlator co-processor that performs chip rate processing. The correlator co-processor performs chip rate processing using a chip correlator 34 (col. 2, lines 49 to 54; col. 3, lines 34 to 50). The DSP (the digital receiver) performs the symbol processing (Fig. 2; col. 5, lines 51 to 60). In other words, Sriram is no different from the prior

art disclosed in the background of the invention. Sriram teaches a receiver 10 having a symbol rate processor 37 performing symbol rate processing and a co-processor 12 performing a chip processing (Fig. 2; col. 3, lines 34 to 50 and col. 4, lines 28 to 42).

In short, Sriram's receiver 10 only performs symbol rate processing function and the co-processor 12 performs the chip rate processing. That is, one processor for each type of processing is provided. In Sriram, the receiver only has a symbol rate processor and the chip rate processing is performed in a separate co-processor. Sriram fails to teach or suggest a receiver with a digital signal processor that can perform both symbol rate and chip rate processing.

Therefore, "at least one digital processor configured to perform a symbol rate processing and at least parts of a chip rate processing," as recited in claim 1, is not disclosed in Sriram, which lacks having a processor configured to perform both types of processing. For at least this exemplary reason, claim 1 is patentably distinguishable from (and is patentable over) Sriram. Therefore, Applicant respectfully requests the Examiner to withdraw this rejection of claim 1. Claims 6-8 are patentable at least by virtue of their dependency on claim 1.

Independent claims 9-12 recites features similar to the features argued above with respect to claim 1. Namely, independent claims 9-12 recite some variation of a digital signal processor configured to perform a symbol rate processing and a chip rate processing.

Claims Rejections under 35 U.S.C. § 103

Claims 2, 3, 13, 14, and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram in view of U.S. Patent No. 4,827,499 to Warty (hereinafter "Warty") and claims 4, 5, and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram and Warty

in view of U.S. Patent No. 6,161,024 to Komara (hereinafter "Komara"). Applicant respectfully traverses these rejections in view of the following comments.

Of these rejected claims 2, 3, 13, 14, and 16, claims 2 and 3 depend on claim 1 and claims 13, 14, and 16 depend on claim 12. Applicant has already demonstrated that Sriram fails to teach or suggest at least a digital signal processor configured to perform a symbol rate processing and at least parts of a chip rate processing. Warty is cited only for its teachings of processors performing task allocation (see page 4 of the Office Action). Clearly, Warty does not cure the deficient teachings of Sriram. Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved the subject matter of claims 1 and 12. Since claims 2, 3, 13, 14, and 16 dependent upon claim 1 or 12, they are patentable at least by virtue of their dependency.

In addition, dependent claim 2, for example, recites: "the signal processor is also configured to perform a task allocation for controlling the chip rate processing and the symbol rate processing." The Examiner acknowledges that Sriram fails to teach or suggest at least this feature of claim 2. The Examiner, however, alleges that Warty cures the deficient teaching of Sriram. In particular, the Examiner alleges that col. 5, lines 36 to 55 of Warty disclose a processor also performing task allocation for controlling the chip rate processing and the symbol rate processing (see page 4 of the Office Action). Col. 5, lines 36 to 55 of Warty recites:

> In such a system, the call assignment, data base and voice channel assignment tasks are initially assigned to specific processors. A percentage of the call control load is then allocated to each of the individual processors at initialization time, based on the load for that processor for other tasks such as call assignment, data base, and voice channel assignment. If overload is detected for any processor, the percentage load for that processor is

> reduced and the percentage load for other processors correspondingly increased. Then, as the overload disappears, the load for that processor is gradually increased until it is back to the initialized load. If any processor fails, its call assignment, data base and voice channel assignment tasks are reassigned to other processors and the call control load percentage is reassigned for each processor. The allocated call control processor load percentage is used to control allocation of calls to the different call control processors, so that, for example, a processor with a 25 percent allocation would receive every fourth call being assigned by a call assignment processor. However, to simplify call processing, calls to directory numbers already assigned to a call control processor are assigned to that processor without regard to the allocation percentage.

As is clear from the passage above, Warty teaches having <u>a separate processor performing allocation of calls</u>. That is, in Warty, the processor <u>is not configured to also allocate tasks in addition to performing chip rate and symbol rate processing</u>. Instead, in Warty, <u>a number of processors are provided to execute a distributed network</u>. Furthermore, in Warty, the separate processor allocates calls and not the control of the chip rate and symbol rate processing.

Moreover, one of ordinary skill in the art would not have been motivated to combine the references in the manner suggested by the Examiner. A critical step in analyzing the patentability of claims pursuant to section 103(a) is ***casting the mind back to the time of invention***, to consider the thinking of one of ordinary skill in the art, ***guided only by the prior art references and the then-accepted wisdom in the field***. *See In re Kotzab*, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (*citing In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)), (emphasis added). Close adherence to this methodology is especially important in cases where the very ease with which the invention can be understood may prompt one "to fall victim to the insidious effect of a hindsight syndrome wherein that which only the invention

taught is used against its teacher." *Kotzab,* 55 USPQ2d at 1316 (*quoting W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 313 (Fed. Cir. 1983)).

Most if not all inventions arise from a combination of old elements. *In re Kotzab*, 55 USPQ2d at 1316 (*citing In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed. Cir. 1998), (emphasis added). Thus, every element of a claimed invention may often be found in the prior art. *Id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *Id.* Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. *In re Kotzab*, 55 USPQ2d at 1316 (*citing In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); and *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

Although a reference need not expressly teach that the disclosure contained therein should be combined with another, ***the showing of combinability, in whatever form, must nevertheless be "clear and particular"***. *Winner International Royalty Corporation v. Ching-Rong Wang* , 202 F.3d 1340, 1348, 53 USPQ2d 1580, 1586-87 (Fed. Cir. 2000), (emphasis added). In the present case, there is no motivation to combine the references in the manner suggested by the Examiner.

To begin, Warty teaches a distributed network for performing control of the communication. That is, Warty notes the problem of inefficiency when only one processor performs administrative functions and allocation of the communication resources (col. 1, lines 15 to 40). Therefore, Warty attempts to improve the allocation and control of the communication

resources in the distributed processing environment by having a number of processors perform administrative functions (col. 2, lines 1 to 30). In other words, Warty's teachings can be seen as an antithesis of the features recited in claim 1. Warty teaches providing a plurality of processors and not a processor configured to perform different types of processing and allocation of tasks. That is, Warty fails to teach or suggest a processor also configured to perform a task allocation for controlling the chip rate processing and the symbol rate processing. Moreover, one of ordinary skill in the art confronted with the problem of power consumption in correlation processing, as addressed by Sriram, would never have turned to Warty, which attempts to improve the call control in a distributed communication switching system. For at least these addition reasons, dependent claim 2 is patentable over the combined teachings of Sriram and Warty.

Next, the rejected claims 4 and 5 depend on claim 1 and claim 15 depends on claim 12. Applicant has already demonstrated that the combined teachings of Sriram and Warty fail to teach or suggest at least a digital signal processor configured to perform a symbol rate processing and at least parts of a chip rate processing, as set forth in the independent claims 1 and 12. Komara is only cited for its teachings of a group of digital processors (see page 5 of the Office Action). Clearly, Komara does not cure the deficient teachings of Sriram and Warty. Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved the subject matter of claims 1 and 12. Since claims 4 and 5 dependent upon claim 1 and claim 15 depends on claim 12, they are patentable at least by virtue of their dependency.

<u>New Claims</u>

In addition, in order to provide more varied protection. Applicant adds claims 19-21. Claim 19 is patentable at least by virtue of its dependency on claim 11. Claim 20 is patentable at least by virtue of its recitation of a digital signal processor having means for performing chip rate processing and symbol rate processing and claim 21 is patentable at least by virtue of its dependency on claim 20.

<u>Conclusion</u>

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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